NEWS RELEASE

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Virage Logic's 45nm and 28nm SiWare™ Memory Compilers Automatically Support Calypto's PowerPro® MG tool

Compilers automatically generate PowerPro MG views to fully automate on-chip memory power optimization

SANTA CLARA, Calif. — February 1, 2010 — Calypto® Design Systems Inc. (www.calypto.com), the leader in sequential analysis technology, today announced that Virage Logic's 45-nanometer (nm) and 28nm SiWare™ Memory compilers now automatically generate PowerPro® MG power optimization models for reducing System-on-Chip (SoC) embedded memory power. This support is the result of a close, ongoing collaboration between the two companies to dramatically reduce on-chip SoC memory power. Using PowerPro MG, designers can reduce both dynamic and leakage memory power, resulting in up to 80 percent memory power reduction compared to previous implementations.

"We are working with Calypto to maximize the opportunity for on-chip memory power savings and enable designers to very easily take advantage of the low-power modes offered by Virage Logic's industry-leading SiWare Memory compilers," said Brani Buric, executive vice president, marketing and sales, of Virage Logic. "The combination of PowerPro MG and our SiWare Memory products allows us to deliver a fully automated, world-class solution to our customers, enabling them to produce the most power-efficient designs possible in the most advanced process nodes available."

Virage Logic delivers memory compilers that enable SoC designers to explore the tradeoffs between performance, area, power and statistical yield to generate optimal memory configurations. The

latest release of the 45nm and 28nm SiWare Memory compliers will now automatically generate PowerPro MG models. This enables design teams to easily integrate PowerPro MG into their fully automated design flows to reduce both dynamic and leakage memory power.

"Power remains the number one SoC design consideration today and on-chip memory power can account for up to 70 percent of the power consumed in an SoC," said Tom Sandoval, chief executive officer of Calypto. "The automatic creation of the PowerPro MG memory model by Virage Logic's SiWare Memory compilers is a great example of how innovative companies are working together to solve some of the most difficult problems SoC designers face."

Using Calypto's patented sequential analysis technology, PowerPro MG constructs new memory gating logic that works in conjunction with the low-power memory modes to produce the lowest power memory implementation possible. PowerPro MG then generates new power-optimized RTL that looks identical to the original RTL except for the addition of the new memory gating logic. PowerPro MG reduces dynamic power by automatically generating logic that controls the memory enable signal and eliminates unnecessary memory accesses. PowerPro MG reduces leakage power by automatically generating logic that controls the sleep modes of individual embedded memories.

Pricing and Availability

Available now, Calypto's PowerPro MG runs on PC platforms running Linux and is priced at $295K for a one year time based license.

About Virage Logic's SiWare Memory Product Portfolio

Virage Logic's SiWare Memory product line provides the world's most area, performance, power, and yield-optimized memories for 65nm, 45nm and below process nodes. The SiWare Memory product portfolio delivers the smallest area and highest performance for a wide range of applications such as wireless, graphics, and high-performance ASICs. These

memory compilers have state-of-the-art power management features to achieve the lowest static and dynamic power consumption.

About Calypto

Founded in 2002, Calypto® Design Systems, Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class power optimization and functional verification software, based on its patented sequential analysis technology. Calypto, whose customers include Fortune 500 companies worldwide**,** is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor program, Si2 and is an active participant in the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America. Corporate headquarters is located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. More information can be found at: www.calypto.com.

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