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NEWS RELEASE

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STARC Adopts Calypto's PowerPro® MG in their STARCAD-CEL Version 4.0 Design Flow

Consortium's Evaluation Demonstrates over 40 Percent Reduction in Memories' Dynamic Power Using PowerPro MG

SANTA CLARA, Calif. and SHIN-YOKOHAMA, Japan — April 12, 2010 **—** Calypto® Design Systems Inc., the leader in sequential analysis technology, today announced that the Semiconductor Technology Academic Research Center (STARC) has adopted Calypto's PowerPro MG product for their STARCAD-CEL Version 4.0 design flow. STARC is a research consortium co-founded by major Japanese semiconductor companies. PowerPro MG automatically reduces both dynamic and leakage memory power in SoCs, and STARC made the decision after completing an extensive evaluation of the tool.

"Designers face significant pressure to reduce power in their designs, and until now, they have not had access to tools that can reduce memory power without requiring extensive, time-consuming analysis and error-prone manual modifications to the design," said Nobuyuki Nishiguchi, Vice President, General Manager, Development Department-1 at STARC. "PowerPro MG surpassed our initial goal to reduce dynamic memory power by 10 percent, delivering a reduction of over 40 percent. It is a tool that companies need to deliver the lowest power SoCs possible."

PowerPro MG also delivered over 60 percent memory leakage power reduction by using a low leakage power mode called light sleep, which is enabled using a single pin. In both cases, SLEC Pro was then used to verify comprehensive equivalence between the original RTL design and the PowerPro MG-optimized RTL design.

"With memory power accounting for up to 70 percent of SoC power, PowerPro MG fills a critical gap in today's power optimization methodolgies for SoC design," says Eiki Suzuki, President of Calypto KK. "The STARC results demonstrate that PowerPro MG dramatically improves the ability of designers to create the most competitive, low-power devices possible."

About PowerPro MG

Using Calypto's patented sequential analysis technology, PowerPro MG takes advantage of the low-power control options available in today's on-chip memories to reduce both dynamic and leakage memory power with little or no impact to timing or area. PowerPro MG reduces dynamic power by automatically generating logic to control the memory enable signal to eliminate unnecessary memory accesses. PowerPro MG reduces leakage power by automatically generating logic to control the sleep modes of individual embedded memories.

About Calypto

Founded in 2002, Calypto® Design Systems, Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class power optimization and functional verification software, based on its patented sequential analysis technology. Calypto, whose customers include Fortune 500 companies worldwide**,** is a member of the Cadence Connections Program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor Program, Si2 and is an active participant in the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America. Corporate headquarters is

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