

## ***NEWS RELEASE***

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### **Calypto's PowerPro CG Selected by AMD to Reduce Power in Processor Designs** *PowerPro CG Improves Performance Per Watt Under Peak Operating Conditions*

**SANTA CLARA, CALIF. — August 4, 2008 —** Calypto™ Design Systems

Inc., the leader in sequential analysis technology, said today that AMD (NYSE: AMD) has selected PowerPro CG (for clock gating) to help optimize power consumption in its next generation of AMD visual media processors.

AMD chose PowerPro CG because of its unique ability to reduce power under peak operating conditions, thus helping to improve the performance-per-watt in its high-performance, energy-efficient and visually realistic solutions. A leader in energy-efficient design, AMD selected PowerPro CG after evaluation on multiple designs and applications.

“The ease-of-use of the PowerPro CG RTL clock gate optimization provided our engineers with the ability to identify opportunities to improve clock gating with minimal effort,” says David Hui, fellow, Silicon Engineering, AMD. “PowerPro CG demonstrates

the impressive power optimization capabilities and results appropriate for use on future AMD designs.”

PowerPro CG, based on Calypto’s patented Sequential Analysis Technology, helps reduce peak and total dynamic power. PowerPro CG evaluates circuit behavior across multiple clock cycles to identify and insert sequential clock gating enable logic into the original RTL code while maintaining all user defined pragmas and comments. PowerPro CG consistently produces better results in significantly less time than manual clock gating.

”AMD is a recognized leader in energy-efficient processing solutions and a long time customer of Calypto products,” adds Mitch Dale, marketing director of Calypto Design System. “We are pleased to be working with AMD on today’s foremost low power design flow.”

### **About Calypto**

Founded in 2002, Calypto Design Systems, Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class power optimization and functional verification software, based on its patented sequential analysis technology. Calypto, whose customers include Fortune 500 companies worldwide, is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program and the Mentor Graphics OpenDoor program. Calypto has offices in Europe, India, Japan and North America. Corporate Headquarters is located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. More information can be found at: [www.calypto.com](http://www.calypto.com).

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