

NEWS RELEASE

Calypto Continues Focus on Technology Leadership with Appointments of New Technology Advisory Board Members

*Pioneers in formal verification and sequential design
further strengthen advisory group*

SANTA CLARA, Calif., August 10, 2005 - Calypto Design Systems, Inc., the technology leader bridging system- and register-transfer-level (RTL) design, today announced the appointment of two new members to the company's technology advisory board (TAB): Dr. Edmund Clarke, FORE Systems Professor of Carnegie Mellon University's School of Computer Science, and Dr. Farid Najm, professor and vice chair of the University of Toronto's Electrical and Computer Engineering (ECE) department. Dr. Clarke, a pioneer in formal verification, and Dr. Najm, an authority in power analysis and high-level modeling, join an advisory board that includes both industry and academic leaders.

Dr. Clarke is considered to be a pioneer in formal verification. His research in 1981 led the way for the use of model checking in hardware verification. He has also received an ACM Kanellakis Award for the development of symbolic checking and an IEEE Harry H. Goode Memorial Award for significant and pioneering contributions to formal verification of hardware and software systems.

An IEEE Fellow, Dr. Najm has made seminal contributions over the last 15 years to practical techniques for modeling and estimation. His pioneering work on static techniques for

power analysis and high-level modeling are part of industrial practice today. His current research is focused on emerging problems in the areas of power, timing, and variability.

"Calypto continues to invest heavily in the expertise, technology, and methodology needed to help designers fully capitalize on the benefits of high-level design," said Devadas Varma, CEO of Calypto Design Systems. "We're delighted Dr. Clarke and Dr. Najm will lend us their decades of expertise to not only help us speed the industry's migration to higher levels of design abstraction, but also address the difficult verification challenges of today."

"Calypto has started on a very innovative technology path that solves real customer problems," stated Dr. Clarke. "I'm pleased to join Calypto's TAB and contribute to their technology direction."

"One of the next shifts in design is to utilize sequential changes to meet timing and power requirements," said Dr. Najm. "I'm looking forward to close collaboration with Calypto to meet the verification challenges of these sequential changes."

As designers move to higher levels of abstraction, Calypto's technology and SLEC family of products help ensure a match between RTL and high-level design implementations. Calypto's SLEC also verifies the functional equivalence between two versions of an RTL design. Calypto's technology advisory board was formed in 2003 to provide Calypto's engineering and methodology teams with appropriate technology direction and feedback from both the academic and end-user sides. Other members of the Calypto TAB include Dr. Magdy Abadir, Freescale Semiconductor, Bruce Beers, previously with IBM Microelectronics, Dr. Tim Cheng, UCSB, Dr. Masahiro Fujita, University of Tokyo, and Dr. Rajesh Gupta, UCSD.

About Calypto

Founded in 2002, Calypto Design Systems, Inc. enables IC design teams to bridge system and RTL for semiconductor design, thereby saving millions of dollars in design costs and silicon re-spins. The company delivers software products to leading edge semiconductor and systems companies worldwide. Calypto is privately held with venture funding from Cipio Partners, JAFCO Ventures, Tallwood Venture Capital and Walden International. The company is a member of the Cadence Connections program, the IEEE-SA, the Open SystemC Initiative (OSCI), Synopsys SystemVerilog Catalyst Program, and the Mentor Graphics OpenDoor program. More information about the company may be found at www.calypto.com.

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