NEWS RELEASE

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Calypto's Sequential Equivalence Checking Product Supports New Cadence C-to-Silicon Compiler

SLEC System-HLS Offers Comprehensive Formal Verification for Algorithm-to-RTL Equivalency Checking

SANTA CLARA, CALIF. — July 14, 2008 — Calypto™ Design Systems, the leader in sequential analysis technology, today unveiled a new version of its SLEC System-HLS (High Level Synthesis) product that is fully integrated with Cadence® Design Systems' new C-to-Silicon Compiler high-level synthesis technology.

Calypto and Cadence joined forces to deliver a dynamic, system-level design solution that dramatically increases designer productivity by automating the C-to-Silicon Compiler and SLEC (Sequential Logic Equivalence Checker) verification flow. SLEC System-HLS, based on Calypto's patented sequential analysis technology, verifies that the register transfer level (RTL) code generated by C-to-Silicon Compiler is functionally equivalent to the original SystemC code.

"The industry requires formal equivalence checking in high-level synthesis flows" states Hisaharu Miwa, general manager of Design Technology Division, LSI Product Technology Unit, Renesas Technology Corp., whose design team was an early adopter of the integrated Cadence/Calypto flow. "We found that the Calypto SLEC System-HLS and Cadence C-to-Silicon Compiler integration provides us an excellent system-level formal verification flow, saving our design team significant time and maximizing productivity."

SLEC is the semiconductor industry's only functional verification solution to formally verify equivalence between electronic system level (ESL) models and RTL implementations. SLEC System-HLS comprehensively verifies the output of C-to-Silicon Compiler, eliminating the need for many time-consuming simulation regressions.

"Calypto's SLEC System-HLS product has become the standard for system-level equivalence checking," said Michael McNamara, VP/GM of the Cadence C-to-Silicon Compiler technology incubator. "Adding a tight integration between SLEC System-HLS and C-to-Silicon Compiler to our design and verification flows built around both the Encounter® digital IC design and Incisive® verification platforms enables Cadence to provide customers with a comprehensive solution for system level design and verification."

Calypto will demonstrate the integration between SLEC System-HLS and C-to-Silicon Compiler at the Cadence CDNLive! user conference this week in Tokyo, Japan. For more information, go to http://www.cadence.com/cdnlive/.

Pricing and Availability

SLEC System-HLS is an added option to SLEC System. SLEC System-HLS tightly integrates SLEC System into HLS design flows and includes solutions for Cadence Design Systems' C-to-Silicon Compiler, Forte Design Systems' Cynthesizer™ and Mentor™ Graphics' Catapult-C. Each HLS vendor solution is sold separately and priced at $50,000 for a one-year, time-based license.

For more information, visit Calypto's website at: www.calypto.com.

About Calypto

Founded in 2002, Calypto Design Systems, Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class power optimization and functional verification software, based on its patented sequential analysis technology. Calypto, whose customers include Fortune 500 companies worldwide**,** is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor program and the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America. Corporate Headquarters is located at: 2933Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. More information can be found at: www.calypto.com.

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