Mentor Graphics Addresses 28nm and 3D-IC Requirements in TSMC Reference Flow 12

WILSONVILLE, Ore., June 2, 2011 - Mentor Graphics Corporation (NASDAQ: MENT) today announced the inclusion of Mentor® system and IC design and implementation for TSMC's Reference Flow 12 targeting TSMC 28nm process technology. New Mentor capabilities in the TSMC Reference Flow include the expanded use of ESL and functional verification tools for full SoC design, extensions to the Olympus-SoC™ place and route system for advanced node routing, DFM, improved yield, and low power designs. Other additions include new 3D-IC verification and testing capabilities in the Calibre® and Tessent® platforms, the Hyper Lynx® simulation of silicon interposer designs for Wide-Bus memory stacks, and new DFM-aware yield analysis using the Calibre and the Tessent YieldInsight® products.

"Collaborating to deliver complete TSMC 28nm design infrastructure, Mentor continues to evolve its comprehensive design and implementation flow to meet the needs of our mutual customers creating designs at the 28nm process node," said Suk Lee, director of Design Infrastructure Marketing at TSMC. "In addition, Mentor's current 3D-IC physical verification and testing enables our customers to take advantage of vertical scaling without disruptive changes to their working methods or tool flow, and provides a roadmap for expanded capabilities as the 3D-IC market advances."

Digital Design for 28nm The Olympus-SoC place and route system provides comprehensive support for TSMC 28nm routing rules, extensions to stage-based OCV to account for process and temperature variation, and electro migration (EM) aware clock tree cell synthesis to minimize hotspots by considering tile-based power budgets along with timing. Resistance aware optimization minimizes wire resistance to improve timing, and cell-based setup/hold uncertainty accounts for cell-specific variation to maximize performance.

The Olympus-SoC system now has the ability to use the Calibre pattern matching capabilities to identify and fix yield detracting patterns. In addition, critical path aware dummy fill identifies critical nets in the GDS and avoids metal fill in those areas to help maintain QoR. For power optimization, multi-corner multi-mode (MCMM) aware leakage analysis concurrently minimizes worst case leakage and improves timing in multi-Vt designs. Low power clock flop placement uses clustering to minimize capacitance in clock leaf buffers, reducing power without impacting timing.

The Calibre PERC product now supports the RF12.0 Charged Device Model (CDM) ESD protection scheme using combined netlist-topological checking to verify protection circuits between driver and receiver gates on nets crossing cross power domains.

Electronic System Level Design and Verification The Mentor electronic system level (ESL) design and verification flow now addresses full SoC designs with support for transaction level model (TLM) based Virtual Platforms enabling early software validation, power estimation and model reuse and refinement to RTL. The Vista™ platform supports functional validation and power estimation based on TSMC iPPA process node value characterization, and enables OS booting and early validation of application software on a Virtual TLM Platform. The Certe™ Testbench Studio product provides automated Universal Verification Methodology (UVM) testbench creation, saving time and reducing errors. The Catapult® C high-level synthesis tool supports SystemC and incremental synthesis, which is demonstrated on a complete, multi-block, hardware accelerator component. The Catapult C tool's generated RTL, including AXI interfaces, is combined with the Questa® Verification IP and a TLM Virtual Platform running in Vista to provide a hybrid TLM and RTL simulation. The Questa Ultra Platform provides an ESL to RTL verification flow with UVM that supports TLM platform and model reuse, test plan tracking and accelerated coverage closure. Questa Codelink provides HW/SW co-verification to greatly reduce debug time when running system tests on an embedded processor.

Tessent IC Test and Yield Analysis The Calibre platform DFM capabilities have been more tightly integrated with the Tessent Diagnosis and the Tessent YieldInsight products to further extend the ability to understand and identify yield loss from scan test data. DFM violations are overlaid with layout-aware diagnosis results to identify if yield loss is associated with DFM yield limiting layout features and to help quantify expected yield entitlement.

Custom IC Design The IC Station platform now addresses layout dependency effect (LDE) predictions during device placement before routing with 'on the fly' LDE assessment from a MOS calculator instead of a spice simulator to shorten design cycle time.

"Mentor's complete system-to-silicon track in Reference Flow 12.0 addresses the biggest challenges in SOC design, from the system level all the way through physical design, verification and single and multi-die package testing," said Walden C. Rhines, chairman and CEO, Mentor Graphics. "Our close collaboration with TSMC allows us to deliver a continuous stream of new technology that is highly optimized to enable foundry customers to get maximum value from advanced manufacturing processes while meeting their time to market objectives."

About Mentor Graphics Mentor Graphics Corporation (NASDAQ: MENT) is a world leader in electronic hardware and software design solutions, providing products, consulting services and award-winning support for the world's most successful electronic, semiconductor and systems companies. Established in 1981, the company reported revenues over the last 12 months of about $915 million. Corporate headquarters are located at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777. World Wide Web site: http://www.mentor.com/.

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