NEWS RELEASE

Calypto's SLEC™ Sequential Equivalence Checker Deployed by Freescale Semiconductor PowerPC Team

Breakthrough verification tool in production use for microprocessor design

SANTA CLARA, Calif. - June 10, 2005 - Calypto Design Systems, Inc., the technology leader bridging system and register-transfer-level (RTL) design, today announced that it plans to provide The PowerPC® core development team at Freescale Semiconductor, Inc. with its SLEC™ product family. Freescale is using the functional verification product for application in its e700 processor platform, containing a PowerPC core and design flow.

"Having SLEC in our design process gives our team flexibility when optimizing RTL," stated John Arends, director of PowerPC core development at Freescale. "In designing our next-generation e700 core, we employ a process of iterative refinement from high-level RTL specification to detailed implementation. This technology is especially helpful in meeting the timing goals of a high performance design. Leveraging all the existing stimulus-based verification cycles that we ran on logic during the pre-timing-closure phase, SLEC enables us to confidently close timing."

Freescale offers a broad range of leading-edge processors for automotive, consumer electronics, networking and wireless communications applications with compelling price/performance ratios for exacting power and performance requirements. "The PowerPC

group at Freescale is a valued customer," said Devadas Varma, CEO of Calypto. "Together we have established a comprehensive verification methodology for leading edge processor design based on SLEC."

The SLEC product family is the industry's first commercially available sequential equivalence checker. SLEC proves functional equivalence between designs that contain differences in levels of sequential and data abstraction. SLEC can verify functional equivalence for difficult-to-verify microarchitectural and timing changes such as pipelining, timing re-balancing, resource-sharing, and designs with different interfaces. The product family initially includes two products: SLEC SYSTEM and SLEC RTL. SLEC SYSTEM is used by design teams to check that RTL implementations match a system-level design, while SLEC RTL checks functional equivalence between two versions of an RTL design that have dramatically different architectures and timing.

About Calypto

Founded in 2002, Calypto Design Systems, Inc. enables IC design teams to bridge system and RTL for semiconductor design, thereby saving millions of dollars in design costs and silicon re-spins. The company delivers software products to leading edge semiconductor and systems companies worldwide. Calypto is privately held with venture funding from Cipio Partners, JAFCO Ventures, Tallwood Venture Capital and Walden International. The company is a member of the Cadence Connections program, the IEEE-SA, the Open SystemC Initiative (OSCI), Synopsys SystemVerilog Catalyst Program, and the Mentor Graphics OpenDoor program. More information about the company may be found at www.calypto.com.

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