NEWS RELEASE

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Calypto Announces New SLEC Release for Comprehensive Verification of Wireless, Video, Image Processing System-on-Chip Designs Latest Capabilities Support Fixed-Point Datatypes, System-Level Memory Interfaces

SANTA CLARA, CALIF. — November 10, 2008 — Calypto[™] Design

Systems Inc., the sequential analysis technology leader, announced today the latest version of SLEC[™] supports fixed-point datatypes and system-level memory interfaces commonly used in wireless, video and image processing system-on-chip (SoC) designs.

"SLEC is an essential verification solution for design teams developing leading electronic products," says Tom Sandoval, Calypto's chief executive officer. "Calypto has added new capabilities to comprehensively verify the latest high-level synthesis features."

SLEC is the cornerstone of advanced system-level design flows, including those using high-level synthesis (HLS) tools such as Mentor Graphics' Catapult® C and Forte Design Systems' CynthesizerTM. The latest release of SLEC supports ac_fixed and cynw_fixed dataypes which are commonly used in wireless designs to model digital signal processing algorithms such as Fast Fourier Transforms and Reed Solomon decoders. SLEC comprehensively verifies the register transfer level (RTL) implementation generated by HLS without running time consuming simulations.

Similarly, SLEC supports ac_windows and external memory interfaces which simplify system-level modeling of computations on large frames data typical in H.264 codec and edge detection designs.

Used by design teams around the world, SLEC proves the functional equivalence between designs with sequential differences. By verifying that two designs produce the same output for all possible inputs, over all time, the quality of verification that SLEC performs in minutes is equal to years of running simulation. Because SLEC does not require testbenches or assertions, engineers spend significantly less time developing verification environments and more time creating innovative SoC solutions.

Pricing and Availability

The latest release of SLEC is shipping now and runs on Linux.

For more details, contact Calypto at info@calypto.com.

About Calypto

Founded in 2002, Calypto Design Systems Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class power optimization and functional verification software, based on its patented sequential analysis technology. Calypto, whose customers include Fortune 500 companies worldwide, is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor program, Si2 and is an active participant in the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America. Corporate Headquarters is located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. More information can

be found at: www.calypto.com.

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