

## **Greg Orzech Joins Calypto as VP of Worldwide Sales, Supports Company Focus on ESL Hardware Design**

SANTA CLARA, Calif., – October 12, 2011 – [Calypto® Design Systems](#), Inc., the leader in ESL hardware design and RTL power optimization, today announced that Greg Orzech has joined the company as VP of Worldwide Sales. Before joining Calypto, Greg was the VP of Worldwide Field Operations at Intrinsicity.

“With the dramatic increase in ESL adoption by our industry, it became necessary to expand our field operations to better serve our customers,” said Doug Aitelli, Chief Executive Officer at Calypto. “Adding a VP of sales with Greg’s many years of experience in sales and management will keep us on track.”

“Calypto has a unique opportunity to become the ESL hardware design leader in EDA,” added Greg Orzech. “Calypto owns all of the pieces: high level synthesis, sequential equivalence checking and sequential power optimization. Our efforts are focused on making the hardware implementation platforms centered on Catapult, SLEC and PowerPro available for mainstream market adoption.”

Greg joins Calypto with more than 30 years of experience in sales, sales management and executive sales management. Before joining Calypto, he was the VP of Worldwide Field Operations at Intrinsicity. Prior to Intrinsicity, Greg held executive sales management and sales management roles at VA Linux Systems, Synopsys, Tendril Networks, Cadence and National Semiconductor. Greg received his B.S. in Mechanical Engineering from Michigan Technological University.

### **About Calypto’s Products**

[Catapult®](#) High Level Synthesis, Calypto’s [SLEC®](#) (Sequential Logic Equivalence Checking) and [PowerPro®](#) platforms are used by seven out of the top ten semiconductor companies and over 100 leading consumer electronics companies worldwide. Calypto’s products enable electronic system level design by engineers to dramatically improve design quality and reduce power consumption of their system-on-chip (SOC) devices.

### **About Calypto**

[Calypto® Design Systems](#), Inc. is the leader in ESL hardware design and RTL power optimization. Calypto, whose customers include Fortune 500 companies worldwide, is a member of the ARM Connected Community, Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the

Mentor Graphics OpenDoor program, Si2 and is an active participant in the Power Forward Initiative.  
Calypto has offices in Europe, India, Japan and North America.  
More information can be found at [www.calypto.com](http://www.calypto.com).

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Press Contact:

Georgia Marszalek, ValleyPR, LLC for Calypto, +1-650.345.7477, Georgia@ValleyPR.com

Notes to editors:

A photo is available on request.

Acronyms

ESL: Electronic System Level

RTL: Register Transfer Level

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