NEWS RELEASE

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Calypto Expands Industry Lead in ESL Verification with Latest SLEC Release

New Breakthrough in Formal Verification Technology for Complex Loop Handling

SANTA CLARA, Calif. — June 7, 2010 — Enabling electronic system level (ESL) design flows for increasingly complex system on a chip (SoC) devices, Calypto® Design Systems, Inc. (www.calypto.com) today announced that its latest SLEC® 5.0, release includes breakthrough technology for verifying deep, complex loop structures in ESL flows. SLEC is the industry's only comprehensive functional verification solution that formally verifies equivalence between ESL models and RTL implementations.

"The accelerating maturity of ESL flows requires Calypto's R&D team to continuously advance our algorithms to support an expanding set of designs, including those that use loop structures to define complex digital functions," said Tom Sandoval, chief executive officer of Calypto Design Systems. "The technology breakthroughs in SLEC 5.0 will enable the tool to support new application spaces and provide a significantly improved user experience for our customers."

SLEC 5.0 includes next generation formal verification algorithms to handle designs with deep, complex loops. Previous algorithms for loop verification relied on expensive and often prohibitive loop unrolling technique that limited capacity and forced users to manage loop sizes by setting static loop bounds. With Calypto's latest advances, verification of designs with complex loops will no longer require the user to provide constraints, dramatically improving the user experience and delivering a comprehensive and scalable verification solution for a broader set of design applications.

New Features for Handling Designs with Large Memories

SLEC 5.0 also includes new features that enable comprehensive verification of designs with large memories. Large arrays in a system level design that model large memories in the corresponding RTL design can stress the capacity boundaries of formal verification methods.

SLEC 5.0 includes new techniques to model memories that reduce their size in SLEC's database by up to 90 percent and effectively increase the size of the memories that can be handled by SLEC.

Improvements in SLEC System-HLS Flows

SLEC 5.0 includes enhanced flows for the three leading high level synthesis (HLS) products in the market, improving usability and expanding the support of their latest features:

- For Mentor CatapultC: New cat2SLEC flow auto-refines throughput, latency, ac_channel size, flop maps and reset length
- For Cadence C-to-Silicon: New ctos2SLEC flow that utilizes CtoSilicon XML database to auto populate design characteristics required for SLEC Verification
- For Forte Cynthesizer: New cyn2SLEC, fully automated support for external memories and custom interfaces in pipelined designs

SLEC Family of Products

The SLEC family of products includes:

- **SLEC System**: Formally verifies equivalence of system-level models and RTL designs.
- **SLEC System-HLS**: Formally verifies that an RTL design generated using high-level synthesis is functionally equivalent to its corresponding system level model.
- **SLEC RTL:** Formally ensures functional equivalence between a golden RTL model and a corresponding RTL model has been sequentially modified to reduce power or improve performance.
- **SLEC Pro**: Comprehensively verifies that an RTL design generated by Calypto's PowerPro product is functionally equivalent to its corresponding golden RTL model.

SLEC 5.0 Showcased at DAC 2010

Highlighting its full suite of PowerPro and SLEC products, Calypto will demonstrate its SLEC 5.0 at this year's Design Automation Conference (DAC) in booth #286, being held June 14-16th in Anaheim, California. To register for a private demonstration visit: www.calypto.com/events.php.

Additionally, Calypto will present at the panel titled, "What input language is the best choice for high level synthesis?" to be held at 4:30 p.m. on Thursday, June 17th in room 207AB.

Pricing and Availability

Available now, Calypto's SLEC 5.0 runs on PC platforms running Linux. Pricing for a one-year, time-based license is as follows:

SLEC System: $250,000

SLEC System-HLS (add on option to SLEC System): $50,000

SLEC RTL: $175,000

SLEC Pro: $125,000

About Calypto

Founded in 2002, Calypto® Design Systems, Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class RTL power optimization and functional verification software, based on its patented sequential analysis technology. Calypto, whose customers include Fortune 500 companies worldwide**,** is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor program, Si2 and is an active participant in the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America. Corporate headquarters is located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. More information can be found at: www.calypto.com.

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