NEWS RELEASE

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STARC Reduces SoC Design Power with Calypto's Unique PowerPro CG Product
PowerPro CG recommended to member companies for RTL power optimization

Shin-Yokohama, Japan. — February 18, 2008 **—** Calypto™ Design Systems Inc., the leader in sequential analysis technology, today announced that the Semiconductor Technology Academic Research Center (STARC) has adopted Calypto's PowerPro™ CG. STARC, a research consortium co-founded by major Japanese semiconductor companies will recommend PowerPro CG to their member companies for RTL power optimization.

"PowerPro CG's ability to read in RTL design and generate a substantially lower power, functionally equivalent RTL is very impressive," said Nobuyuki Nishiguchi, Vice President, General Manager Development Department-1 at STARC. "We found Calypto's unique Sequential Analysis approach to automating RTL power optimization identified many additional clock-gating opportunities and saved design time.."

By analyzing RTL sequential behavior across multiple clock cycles, PowerPro CG is able to clock gate substantially more registers, for longer durations than traditional

combinational clock gating tools. PowerPro CG automatically identifies and inserts sequential clock gating enable conditions directly into synthesizable RTL code. STARC extensively evaluated PowerPro CG on a multi-media signal processing design. On the synthesizable blocks in this design PowerPro CG reduced register power and clock power by 20% when comparing the PowerPro optimized RTL to the original RTL. These results where measured on the gate-level netlists after low power RTL synthesis.

"There is a clear need for automated RTL power optimization tools." says Eiki Suzuki, President of Calypto KK. "As the STARC work shows, Calypto's PowerPro CG saves substantial power and reduces the effort spent by design teams optimizing for power."

PowerPro CG dramatically reduces power consumption by applying sequential analysis at the register transfer level (RTL) to identify micro-architectural optimizations that result in a lower power circuit. PowerPro CG has been shown to reduce total power by 10% to 60% across multiple applications with little or no change in timing or area. PowerPro CG automates RTL power reduction, providing consistently better results in significantly less time than the error prone, time consuming manual techniques.

About Calypto

Founded in 2002, Calypto Design Systems, Inc. enables SoC design teams to bridge System and RTL for semiconductor design, saving millions of dollars in design costs and silicon re-spins. Enabling ESL, Calypto delivers software products to leading-edge semiconductor and systems companies worldwide. Calypto is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program and the Mentor Graphics OpenDoor program. Corporate Headquarters is located at:

2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. More information about Calypto may be found at: http://www.calypto.com

About STARC

STARC is a research consortium of major Japanese semiconductor companies whose mission is to contribute to the growth of the Japanese semiconductor industry by developing leading-edge system-on-chip (SoC) design technologies. For more information about STARC, please visit http://www.starc.jp/index-e.html.