PowerPro® Platform

Silicon-Proven Platform for Low-Power SOC Design

CALYPTO®

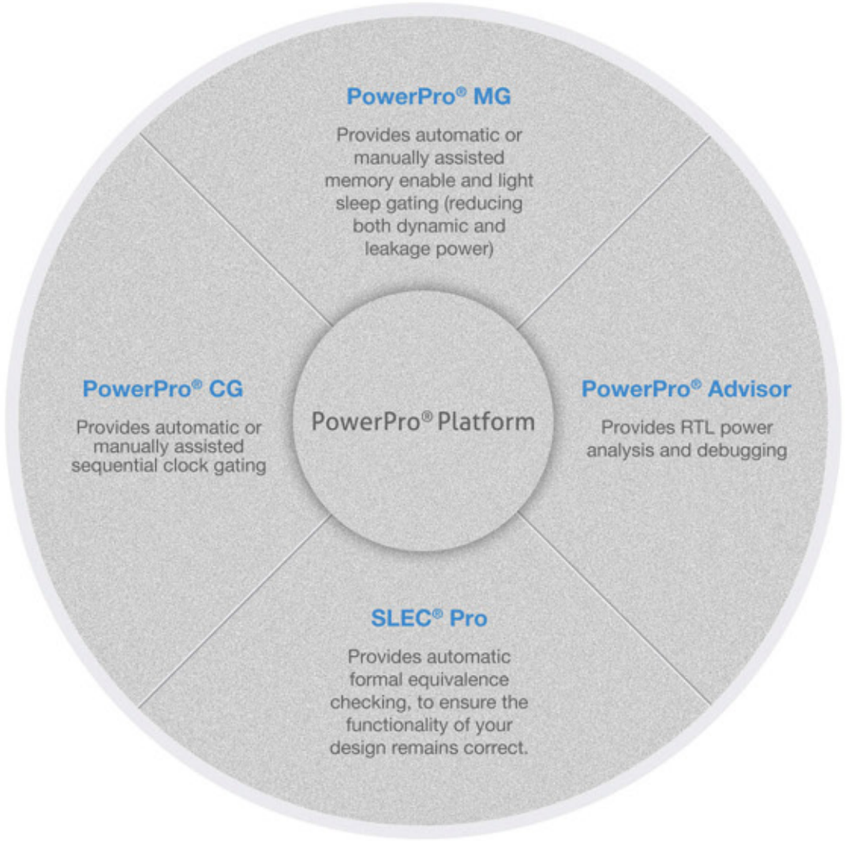
Empowering *the next* level of design

Silicon-Proven Platform for Low-Power SOC Design

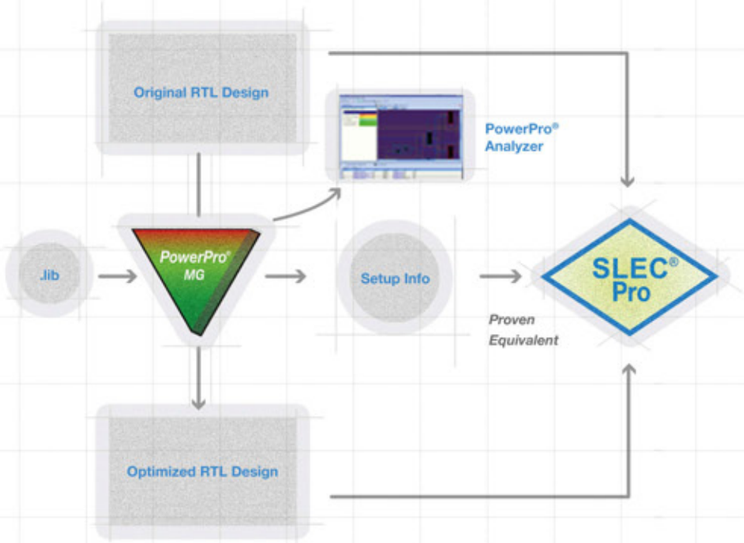
With the explosion of consumer electronics, designing for low-power has become an important design constraint and a key differentiating factor. The RTL design phase provides the ideal opportunity to dramatically reduce power, since several micro-architectural transformations can be done at this stage, both via automated tools as well as manually by the RTL designers. Also, power analysis can be done with reasonable accuracy at the RTL level to drive low power optimizations. Unlike combinational power optimization tools that only work at the gate level, PowerPro operates on the RTL thus giving the user the best opportunity to achieve the lowest power result.

The PowerPro SOC Low-Power Platform is the leading RTL-level, power optimization toolset in the industry. Based on our patented sequential analysis technology, PowerPro looks at a design just like an engineer does, across clock and functional boundaries. Unlike other tools, PowerPro is not based on structural patterns in the design. PowerPro performs a functional analysis across multiple pipeline stages in the design and analyzes the state machines in the design, enabling it to find the most advanced logic conditions possible to shut off redundant sections of a chip. PowerPro can be used to reduce power on the logic, memory, and core processor sections on an SOC.

The PowerPro Platform consists of:



Key Differentiators



Unique Sequential Analysis Technology

Calypto's patented Sequential Analysis Technology allows PowerPro to consistently produce better results by order of magnitude in less time than manual RTL optimizations for power.

Next Generation Prototyping Engine

PowerPro includes the next generation RTL prototyping engine that estimates total power (static and dynamic) accurately thereby allowing the optimal power-performance tradeoff.

Automated RTL generation

PowerPro automates the identification and insertion of sequential gating logic into the user's original RTL to dramatically reduce dynamic and leakage power.

Comprehensive Formal Verification

PowerPro optimized RTL is comprehensively verified with SLEC® Pro to guarantee that no functional changes are introduced.

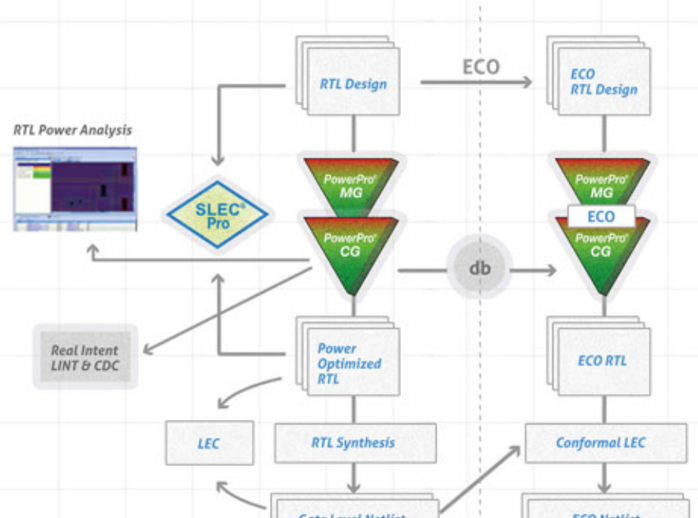
// Additionally, because PowerPro CG maintains cycle-accurate behavior at the block boundary, existing simulation regressions can be used to verify PowerPro CG generated RTL.

Production Proven Flow Features

PowerPro has been used to minimize power of many taped SOC's in the market and has all the features required for supporting downstream implementation and verification.

// ECO
// Automatic synchronizer identification
// Clock-domain aware reset logic insertion
// Customizability of PowerPro RTL to meet customers LINT rules guidelines
// Flow controls for scope of optimization in the design

Integrated into Existing Design Flows



PowerPro is Integrated into Leading RTL Synthesis Tool Flows

All the synthesis pragmas and verification directives are retained in the PowerPro generated RTL for synthesis and simulation.

PowerPro Supports Industry Standard File Formats

// Synthesizable RTL (Verilog, VHDL or SystemVerilog)
// Technology library files (.lib)
// Relevant commands of Synopsys Design Constraints (SDC)
// Switching activity files (SAIF , VCD or FSDB)

PowerPro Works with the Leading CDC and LINT Tool Flows

In addition PowerPro has a tight integration with the Ascent and Meridian products from Real Intent, providing the user a more automated flow.

PowerPro is Controlled through a TCL Interface

The TCL interface is organized into three basic functions: setup, optimize and output.

PowerPro® Family Products

Automatic and manually assisted clock gating

- Reduces logic, clock-tree and register power by cutting of unnecessary toggles at the flop boundary
- Power savings produced by PowerPro CG are complementary and cumulative to downstream power reduction tools used in synthesis, clock tree optimization, and physical design
- Power adviser provides visualization of sequential clock-gating conditions for manual flow

Memory power reduction through memory and light sleep gating

- Reduces dynamic power of the memory by shutting off memory during unnecessary memory accesses
- Reduces leakage power by inserting logic to control power-modes of memory
  - Sequential analysis in PowerPro MG ensures that the memory is taken out of sleep modes adequately before memory access
  - PowerPro MG prototyping technology performs the optimal tradeoff to maximize leakage power savings while minimizing toggling of sleep modes
- Allows flexibility of inserting the memory-gating logic to be inserted in user-driven datapath blocks, thereby preserving the memory hierarchy

RTL power analysis and sequential optimization visualization

PowerPro Analyzer is the industry's most accurate register-transfer level (RTL) power analysis tool:

- Sequential analysis based switching activity propagation engines deliver precise switching activity information for all signals, including internal signals created during prototyping and optimization
- Accurate design prototyping to ensure the design database used for power analysis provides an accurate representation of the final synthesized design
- Advanced clock-gating aware clock-tree synthesis provides accurate clock-tree power
- Power analysis performed using either simulation based design switching activity or PowerPro's vectorless mode
- PowerPro analyzer can provide detailed and hierarchical power reports of dynamic and leakage power consumed by logic, registers, memory and clock-tree
- Power information is reported in the context of RTL source code, schematic display, design hierarchy, and various sortable reports ((ASCII, HTML, CSV, XML) to enable efficient design for low-power

PowerPro Analyzer allows visualization of sequential optimizations for manual optimization of RTL:

- Displays the sequential optimizations as expressions, schematic, reports and embedded in the RTL
- Reports additional optimization potential to reduce power of the SOC
- Interactive and incremental optimization of enable expressions based on designers feedback

System Requirements and Compatibility:

Languages:

VHDL 87, 93 & 97, Verilog 95 & 2001, System Verilog

Operating Systems:

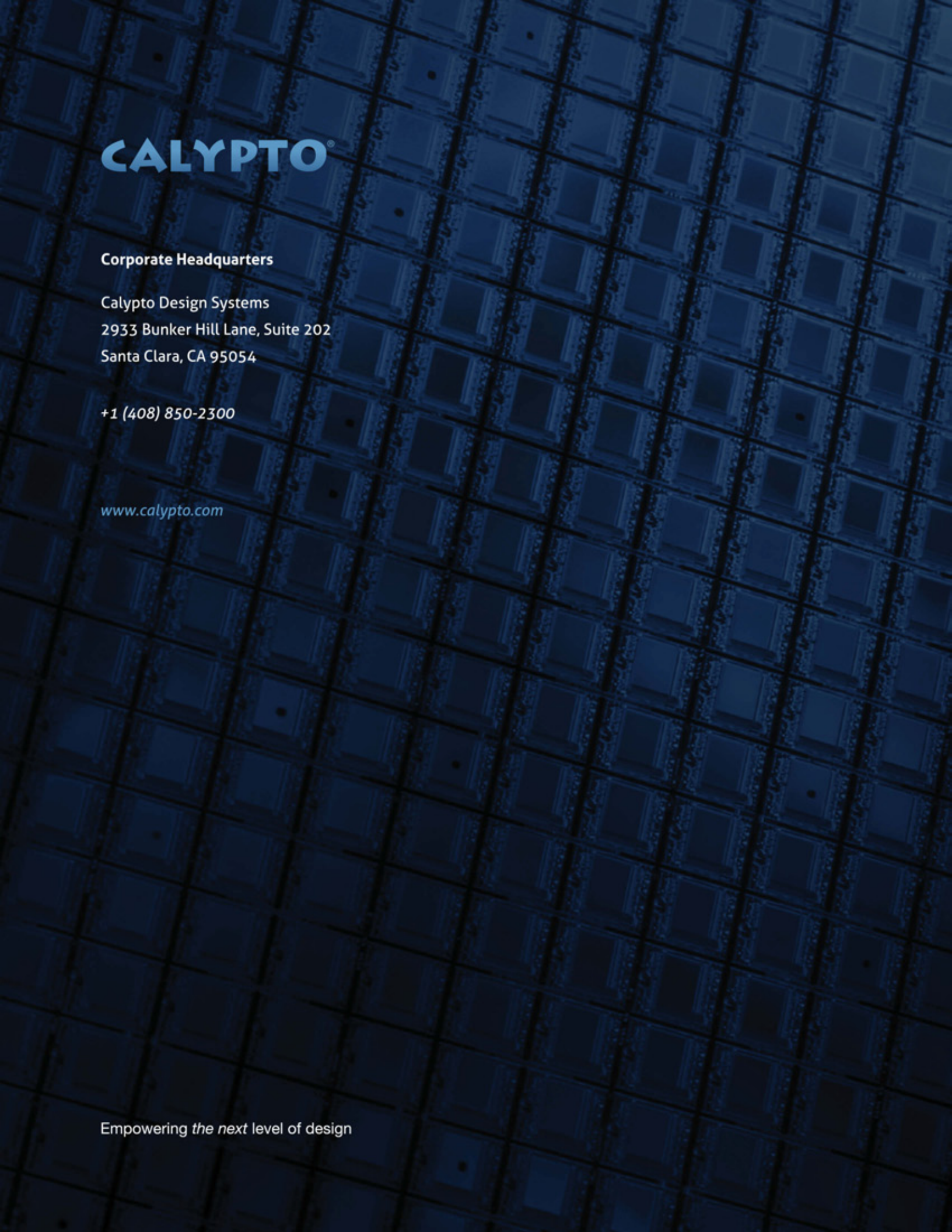
Redhat Enterprise Linux 3.0 and 4.0

Platforms:

32-bit and 64-bit x86 compatible hardware

Memory:

2 GB minimum



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